CLAIMS

1. A monolithic integrated circuit comprising:

an MOS circuit formed at least partially in a monocrystalline substrate;

a monocrystalline compound semiconductor layer overlying the monocrystalline substrate; and

a tunnel diode formed at least partially in the monocrystalline compound semiconductor layer, the tunnel diode electrically coupled to the MOS circuit.

2. The monolithic integrated circuit of claim 1 wherein the MOS circuit comprises an MOS transistor having a drain region and the tunnel diode is electrically coupled to the drain region.

3. The monolithic integrated circuit of claim 2 further comprising a second tunnel diode coupled to the drain region in series with the tunnel diode.

4. The monolithic integrated circuit of claim 1 wherein the MOS circuit comprises an MOS transistor having a drain region and the tunnel diode is formed overlying and electrically coupled to the drain region.

5. The monolithic integrated circuit of claim 1 wherein the MOS circuit comprises an MOS transistor having a gate electrode and the tunnel diode is formed overlying and electrically coupled to the gate electrode.

6. The monolithic integrated circuit of claim 1 wherein the MOS circuit comprises a digital circuit.

7. The monolithic integrated circuit of claim 1 wherein the tunnel diode comprises an interband tunnel diode.

8. The monolithic integrated circuit of claim 1 wherein the tunnel diode comprises an intraband tunnel diode.

9. A semiconductor device comprising:

a monocrystalline semiconductor substrate;

an oxide layer formed overlying the substrate;

a monocrystalline compound semiconductor layer formed overlying the oxide layer; and

a tunnel diode formed at least partially in the monocrystalline compound semiconductor layer.

10. The semiconductor device of claim 9 wherein the tunnel diode comprises an intraband tunnel diode.

11. The semiconductor device of claim 10 wherein the tunnel diode comprises a quantum well layer sandwiched between first and second tunnel barrier layers and the first and second tunnel barrier layers are sandwiched between an injection layer and a collection layer.

12. The semiconductor device of claim 11 wherein the quantum well layer comprises GaAs and the first and second tunnel barrier layers comprise a material selected from AlGaAs and AlAs.

13. The semiconductor device of claim 12 wherein the quantum well layer and the first and second tunnel barrier layers are not intentionally doped.

14. The semiconductor device of claim 12 wherein the injection layer and the collection layer each comprise GaAs.

15. The semiconductor device of claim 14 wherein the injection layer and the collection layer are each impurity doped.

16. The semiconductor device of claim 15 further comprising first and second contact layers contacting the injection layer and the collection layer, respectively, the first and second contact layers comprising monocrystalline GaAs more heavily impurity doped than the injection layer and the collection layer.

17. The semiconductor device of claim 12 further comprising a monocrystalline buffer layer interposed between the oxide layer and the monocrystalline compound semiconductor layer.

18. The semiconductor device of claim 17 wherein the oxide layer comprises an alkali earth metal titanate and the buffer layer comprises a material selected from the group consisting of GaAs and AlGaAs.

19. The semiconductor device of claim 18 wherein the oxide layer comprises $Ba_xSr_{1-x}TiO_3$ where x ranges from 0 to 1.

20. The semiconductor device of claim 12 wherein the oxide layer comprises $Ba_xSr_{1-x}TiO_3$ where x ranges from 0 to 1.

21. The semiconductor device of claim 20 wherein the substrate comprises silicon.

22. The semiconductor device of claim 21 further comprising a digital circuit formed at least partially within the substrate and coupled to the tunnel diode.

23. The semiconductor device of claim 11 wherein the quantum well layer comprises InGaAs and the first and second tunnel barrier layers comprise AlAs.

24. The semiconductor device of claim 23 wherein the injection layer and the collection layer each comprise InGaAs.

25. The semiconductor device of claim 24 further comprising first and second contact layers contacting the injection layer and the collection layer, respectively, the first and second contact layers comprising heavily impurity doped monocrystalline InGaAs.

26. The semiconductor device of claim 24 further comprising a monocrystalline buffer layer between the oxide layer and the monocrystalline compound semiconductor layer.

27. The semiconductor device of claim 26 wherein the buffer layer comprises a material selected from the group consisting of InP and InAlAs.

28. The semiconductor device of claim 27 wherein the oxide layer comprises an oxide selected from the group consisting of alkali earth metal zirconates and alkali earth metal hafnates.

29. The semiconductor device of claim 9 wherein the oxide layer comprises an amorphous oxide layer.

30. The semiconductor device of claim 29 wherein the oxide layer comprises an amorphous oxide formed epitaxially as a monocrystalline oxide layer and subsequently heat treated to convert the monocrystalline oxide to an amorphous oxide.

31. The semiconductor device of claim 9 wherein the tunnel diode comprises an interband tunnel diode.

32. The semiconductor device of claim 31 wherein the tunnel diode comprises first and second quantum well layers spaced apart by a barrier layer and the first and second quantum well layers are sandwiched between first and second carrier supply layers.

33. The semiconductor device of claim 32 wherein the quantum well layers comprise InGaAs and the barrier layer comprises InAlAs.

34. The semiconductor device of claim 33 wherein the quantum well layers and the barrier layer are not intentionally doped.

35. The semiconductor device of claim 33 wherein the first carrier supply layers comprise a layer of n-doped InGaAs and a layer of n-doped InAlAs with the layer of n-doped InAlAs in contact with the first quantum well layer and the second carrier supply layers comprise a layer of p-doped InGaAs and a layer of p-doped InAlAs with the layer of p-doped InAlAs in contact with the second quantum well layer.

36. The semiconductor device of claim 35 further comprising a buffer layer comprising a material selected from the group consisting of InP and InAlAs interposed between the oxide layer and the monocrystalline compound semiconductor layer.

37. The semiconductor device of claim 36 wherein the oxide layer comprises an oxide selected from the group consisting of alkali earth metal zirconates and alkali earth metal hafnates.

38. The semiconductor device of claim 32 wherein the quantum well layers comprise InGaAs and the barrier layer comprises GaAs.

39. The semiconductor device of claim 33 wherein the first carrier supply layer comprises n-doped GaAs and the second carrier supply layer comprises p-doped GaAs.

40. The semiconductor device of claim 39 further comprising a buffer layer comprising GaAs interposed between the oxide layer and the monocrystalline compound semiconductor layer.

41. The semiconductor device of claim 39 wherein the oxide layer comprises an alkali earth metal titanate.

42. The semiconductor device of claim 41 wherein the oxide layer comprises $Ba_xSr_{1-x}TiO_3$ where x ranges from 0 to 1.

43. The semiconductor device of claim 9 wherein the substrate comprises silicon.

44. The semiconductor device of claim 43 further comprising an amorphous silicon oxide formed underlying the oxide layer.

45. The semiconductor device of claim 9 wherein the oxide layer comprises an amorphous oxide formed by heat treating a monocrystalline oxide layer.

46. A process for fabricating a semiconductor device comprising the steps of:

providing a monocrystalline semiconductor substrate;

epitaxially growing a layer of monocrystalline oxide overlying the substrate;

growing a monocrystalline compound semiconductor structure overlying the layer of monocrystalline oxide, the monocrystalline compound semiconductor structure comprising an injection layer, a first tunnel barrier layer, a quantum well layer, a second tunnel barrier layer and a collection layer and

forming an intraband tunnel diode at least partially within the monocrystalline compound semiconductor structure.

47. The process of claim 46 further comprising the step of forming an amorphous oxide layer underlying the layer of monocrystalline oxide during the step of epitaxially growing.

48. The process of claim 47 further comprising the step of thermally annealing the layer of monocrystalline oxide to convert the monocrystalline oxide to a further layer of amorphous oxide.

49. The process of claim 46 wherein the step of growing a monocrystalline compound semiconductor structure comprises the step of growing by a process selected from the group consisting of MBE, MOCVD, CVD, MEE, ALE, PVD, PLD, and CSD.

50. The process of claim of claim 46 wherein the step of providing a semiconductor substrate comprises the step of providing a monocrystalline substrate comprising silicon.

51. The process of claim 50 further comprising the steps of:

forming a digital integrated circuit at least partially within the substrate; and

forming an interconnection electrically interconnecting the digital integrated circuit and the tunnel diode.

52. The process of claim 51 wherein the step of forming a digital integrated circuit comprises the step of forming an MOS transistor having a drain region at the surface of the substrate.

53. The process of claim 52 wherein the step of forming an interconnection comprises the steps of:

selectively ion implanting the layer of monocrystalline oxide overlying the drain region to render the oxide electrically conductive; and

forming the interband tunnel diode in electrical contact with the electrically conductive oxide.

54. A process for fabricating a semiconductor device comprising the steps of:

providing a monocrystalline semiconductor substrate;

epitaxially growing a layer of monocrystalline oxide overlying the substrate;

growing a monocrystalline compound semiconductor structure overlying the layer of monocrystalline oxide, the monocrystalline compound semiconductor structure comprising a first carrier supply layer, a first quantum well layer, a barrier layer, a second quantum well layer, and a second carrier supply layer; and

forming an interband tunnel diode at least partially in the monocrystalline compound semiconductor structure.

55. The process of claim 54 further comprising the step of forming an amorphous oxide layer underlying the layer of monocrystalline oxide during the step of epitaxially growing.

56. The process of claim 55 further comprising the step of thermally annealing the layer of monocrystalline oxide to convert the monocrystalline oxide to a further layer of amorphous oxide.

57. The process of claim 54 wherein the step of growing a monocrystalline compound semiconductor structure comprises the step of growing by a process selected from the group consisting of MBE, MOCVD, CVD, MEE, ALE, PVD, PLD, and CSD.

58. The process of claim 54 further comprising the steps of:

forming a digital integrated circuit at least partially within the substrate; and

forming an interconnection electrically interconnecting the digital integrated circuit and the tunnel diode.

59. The process of claim 58 wherein the step of forming a digital integrated circuit comprises the step of forming an MOS transistor having a drain region at the surface of the substrate.

60. The process of claim 59 wherein the step of forming an interconnection comprises the steps of:

selectively ion implanting the layer of monocrystalline oxide overlying the drain region to render the oxide electrically conductive; and

forming the intraband tunnel diode in electrical contact with the electrically conductive oxide.

61. A process for fabricating a semiconductor device comprising the steps of:

providing a monocrystalline silicon substrate;

forming a CMOS circuit at least partially within the silicon substrate, the CMOS circuit comprising an MOS transistor having source and drain regions and a gate electrode;

epitaxially growing a layer of monocrystalline oxide overlying the substrate;

forming an amorphous layer of silicon oxide underlying the layer of monocrystalline oxide during the step of epitaxially growing;

growing a monocrystalline compound semiconductor structure overlying the layer of monocrystalline oxide;

heat treating the layer of monocrystalline oxide to convert the monocrystalline oxide to an additional layer of amorphous oxide;

forming a tunnel diode at least partially from the monocrystalline compound semiconductor structure; and

forming an electrical interconnection between the tunnel diode and one of the source region, drain region and gate electrode.

62. The process of claim 61 wherein the step of epitaxially growing a layer of monocrystalline oxide comprises the step of epitaxially growing a layer of oxide selected from the group consisting of: alkali earth metal titanates, alkali earth metal hafnates, and alkali earth metal zirconates.

63. The process of claim 62 wherein the step of epitaxially growing a layer of monocrystalline oxide comprises the step of epitaxially growing a layer of $Ba_xSr_{1-x}TiO_3$ where x ranges from 0 to 1.

64. The process of claim 61 wherein the step of forming a tunnel diode comprises the step of etching the monocrystalline compound semiconductor structure to form the tunnel diode directly overlying the MOS transistor.

65. The process of claim 61 further comprising the step of forming a monocrystalline semiconductor buffer layer overlying the layer of monocrystalline oxide and underlying the monocrystalline compound semiconductor structure.

66. The process of claim 65 wherein the buffer layer comprises a material selected from InP, InAlAs, AlGaAs and GaAs.